REMARKS

Claim 20 has been rejected under 35 USC 112(1) for the phrase "testing at integrated cache speeds". Claim 20 has been cancelled, rendering the rejection moot.

Claims 19, 21, 23 and 26 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent 5,483,421 ("Gedney") in view of U.S. patent 5,680,936 ("Beers").

Applicants respectfully traverse these rejections for the following reasons:

The rejection states that Gedney fails to disclose 1) coupling a passive device to the interposer (which also is coupled to the semiconductor die), 2) testing the semiconductor die, 3) coupling the interposer to a substrate if the semiconductor die passes testing, or not coupling it if the semiconductor die does not pass testing. The rejection then relies on Beers to provide the missing elements. However, Beers fails to provide for any of these limitations: 1) Beers does not disclose or suggest coupling a semiconductor and a passive device to an interposer. Beers does not deal with an interposer at all, but rather with a printed circuit board which is not later coupled to a substrate as required by the claims. 2) Beers does not disclose or suggest testing a semiconductor die. Beers tests a completed printed circuit board. At most, the printed circuit board of Beers would contain the integrated circuits that had already been attached to the printed circuit board before Beers begins testing, which is contrary to the claims and which represents the problematic prior art approach that Applicant's invention is intended to overcome. 3) Beers does not couple the tested assembly to anything. Beers separates the tested printed circuit boards into those that passed the testing and those that did not, but does nothing further with the boards. 4) Amended claim 19, and therefore all the remaining claims, recites coupling the interposer to a substrate using solder balls. Beers does not disclose or suggest the use of solder balls. Since the use of solder balls is a technique that is used on integrated circuits but not on printed circuit boards, it would not be obvious to implement this technique on the tested printed circuit boards of Beers.

Gedney and Beers involve completely different devices at completely different stages of the manufacturing process. Combing them in the manner suggested would not

be feasible because the techniques of Gedney are not applicable to the processes of Beers, and the techniques of Beers are not applicable to the processes of Gedney.

CONCLUSION

For the aforementioned reasons, Applicants maintain that claims 19, 21, 23 and 26 are now in condition for allowance. Applicants further maintain that since generic claim 19 is in condition for allowance, claims 22, 24 and 25 should now be considered by the Examiner and found allowable as well. A finding of allowance by the Examiner on claims 19 and 21-26 is therefore respectfully requested. No fee is believed due with this response. In this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOLOKOFF, TAYLOR & ZAFMAN, LLP

Date: 5-3-01

John Travis
Reg. No. 43,203

12400 Wilshire Blvd
Seventh Floor
Los Angeles, California 90025-1026
(512) 330-0844